

MM74HC164 8-Bit Serial-in/Parallel-out Shift Register

Features

- Typical operating frequency: 50MHz
- Typical propagation delay: 19ns (clock to Q)
- Wide operating supply voltage range: 2V to 6V
- Low input current: 1µA maximum
- Low quiescent supply current: 80µA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

General Description

The MM74HC164 utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.


This 8-bit shift register has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip-flop. Inputs A & B permit complete control over the incoming data. A LOW at either or both inputs inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is HIGH or LOW, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

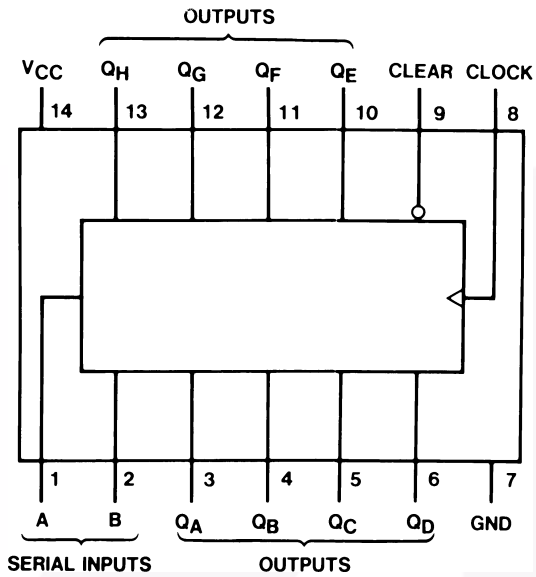
Ordering Information

Order Number	Package Number	Package Description
MM74HC164M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC164MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC164N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Top View

Truth Table

Inputs				Outputs	
Clear	Clock	A	B	Q _A	Q _B ... Q _H
L	X	X	X	L	L ... L
H	L	X	X	Q _{AO}	Q _{BO} ... Q _{HO}
H	↑	H	H	H	Q _{An} ... Q _{Gn}
H	↑	L	X	L	Q _A ... Q _{Gn}
H	↑	X	L	L	Q _{An} ... Q _{Gn}

H = HIGH Level (steady state)

L = LOW Level (steady state)

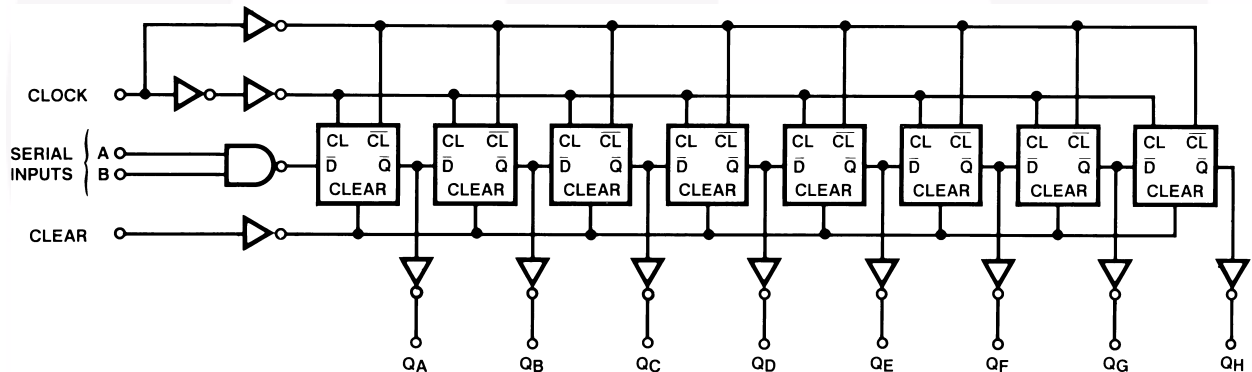
X = Irrelevant (any input, including transitions)

↑ = Transition from LOW-to-HIGH level.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

Logic Diagram



Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5 to +7.0V
V_{IN}	DC Input Voltage	-1.5 to $V_{CC}+1.5V$
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC}+0.5V$
I_{IK}, I_{OK}	Clamp Diode Current	$\pm 20mA$
I_{OUT}	DC Output Current, per pin	$\pm 25mA$
I_{CC}	DC V_{CC} or GND Current, per pin	$\pm 50mA$
T_{STG}	Storage Temperature Range	-65°C to +150°C
P_D	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic “N” package: -12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	-40	+85	°C
t_r, t_f	Input Rise or Fall Times $V_{CC} = 2.0V$		1000	ns
	$V_{CC} = 4.5V$		500	ns
	$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics⁽³⁾

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C		T _A = -40°C to 85°C	T _A = -55°C to 125°C	Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	2.0			1.5	1.5	1.5	V
		4.5			3.15	3.15	3.15	
		6.0			4.2	4.2	4.2	
V _{IL}	Maximum LOW Level Input Voltage	2.0			0.5	0.5	0.5	V
		4.5			1.35	1.35	1.35	
		6.0			1.8	1.8	1.8	
V _{OH}	Minimum HIGH Level Output Voltage	2.0	V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 20μA	2.0	1.9	1.9	1.9	V
		4.5		4.5	4.4	4.4	4.4	
		6.0		6.0	5.9	5.9	5.9	
		4.5	V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 4.0mA	4.2	3.98	3.84	3.7	
		6.0		V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 5.2mA	5.7	5.48	5.34	
V _{OL}	Maximum LOW Level Output Voltage	2.0	V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 20μA		0	0.1	0.1	0.1
		4.5		0	0.1	0.1	0.1	
		6.0		0	0.1	0.1	0.1	
		4.5	V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 4.0mA	0.2	0.26	0.33	0.4	
		6.0		V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 5.2mA	0.2	0.26	0.33	0.4
I _{IN}	Maximum Input Current	6.0	V _{IN} = V _{CC} or GND			±0.1	±1.0	±1.0
I _{CC}	Maximum Quiescent Supply Current	6.0	V _{IN} = V _{CC} or GND, I _{OUT} = 0μA		8.0	80	160	μA

Note:

3. For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15pF, t_r = t_f = 6ns

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
f _{MAX}	Maximum Operating Frequency			30	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock to Output		19	30	ns
t _{PHL}	Maximum Propagation Delay, Clear to Output		23	35	ns
t _{REM}	Minimum Removal Time, Clear to Clock		-2	0	ns
t _S	Minimum Setup Time, Data to Clock		12	20	ns
t _H	Minimum Hold Time, Clock to Data		1	5	ns
t _W	Minimum Pulse Width, Clear or Clock		10	16	ns

AC Electrical Characteristics

$C_L = 50\text{pF}$, $t_r = t_f = 6\text{ns}$ (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C}$	$T_A = -55^\circ\text{C}$	Units
				Typ.	Guaranteed Limits		to 85°C	
f_{MAX}	Maximum Operating Frequency	2.0			5	4	3	MHz
		4.5			27	21	18	
		6.0			31	24	20	
$t_{\text{PHL}}, t_{\text{PLH}}$	Maximum Propagation Delay, Clock to Output	2.0		115	175	218	254	ns
		4.5		13	35	44	51	
		6.0		20	30	38	44	
t_{PHL}	Maximum Propagation Delay, Clear to Output	2.0		140	205	256	297	ns
		4.5		28	41	51	59	
		6.0		24	35	44	51	
t_{REM}	Minimum Removal Time, Clear to Clock	2.0		-7	0	0	0	ns
		4.5		-3	0	0	0	
		6.0		-2	0	0	0	
t_S	Minimum Setup Time, Data to Clock	2.0		25	100	125	150	ns
		4.5		14	20	25	30	
		6.0		12	17	21	25	
t_H	Minimum Hold Time, Clock to Data	2.0		-2	5	5	5	ns
		4.5		0	5	5	5	
		6.0		1	5	5	5	
t_W	Minimum Pulse Width Clear or Clock	2.0		22	80	100	120	ns
		4.5		11	16	20	24	
		6.0		10	14	18	20	
$t_{\text{THL}}, t_{\text{TLH}}$	Maximum Output Rise and Fall Time	2.0			75	95	110	ns
		4.5			15	19	22	
		6.0			13	16	19	
t_r, t_f	Maximum Input Rise and Fall Time	2.0			1000	1000	1000	ns
		4.5			500	500	500	
		6.0			400	400	400	
C_{PD}	Power Dissipation Capacitance ⁽⁴⁾	5.0	(per package)	150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note:

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{\text{PD}} V_{\text{CC}}^2 f + I_{\text{CC}} V_{\text{CC}}$, and the no load dynamic current consumption, $I_S = C_{\text{PD}} V_{\text{CC}} f + I_{\text{CC}}$.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

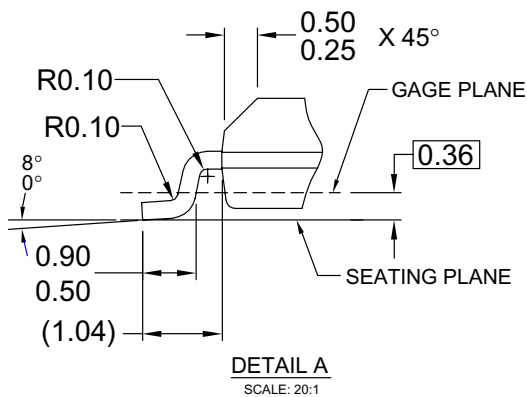


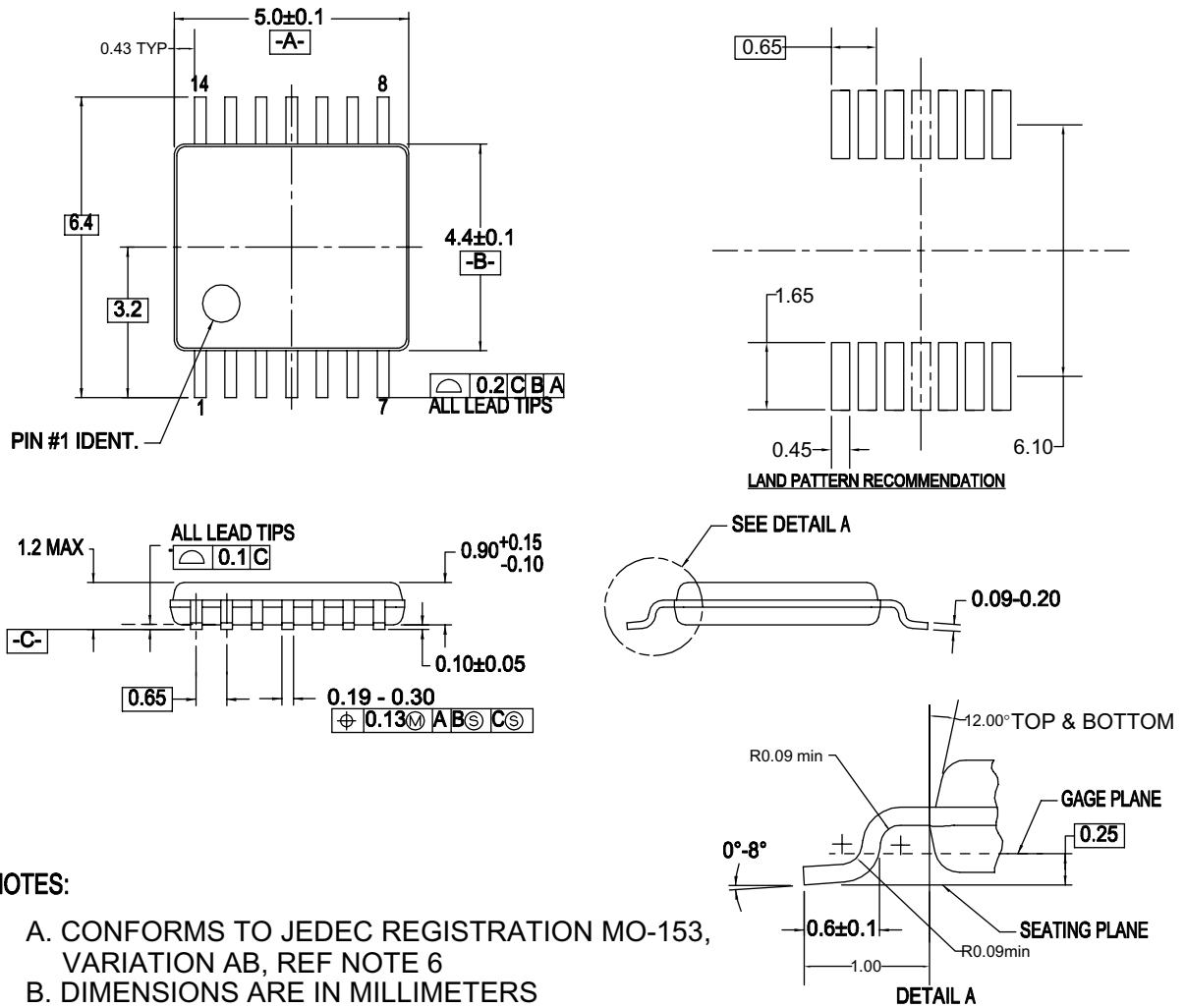
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

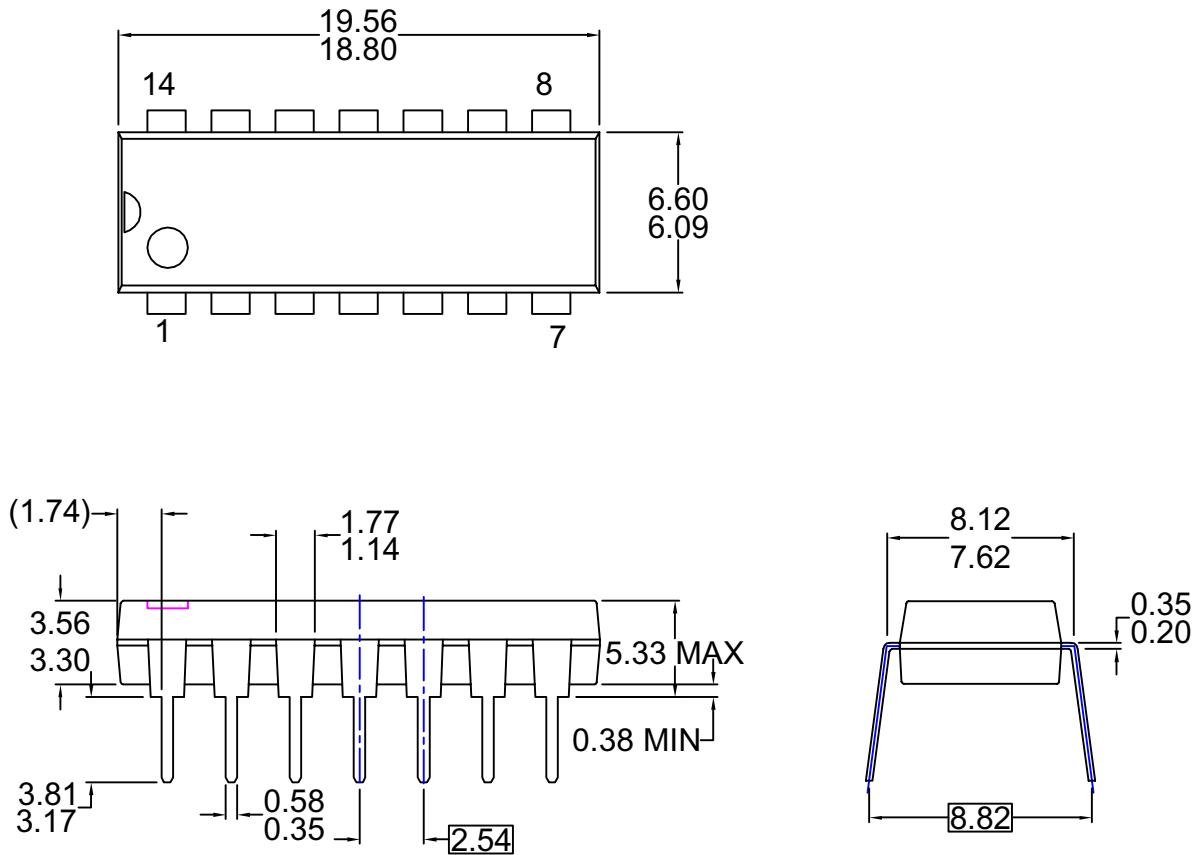
Figure 2. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



- NOTES: UNLESS OTHERWISE SPECIFIED**
THIS PACKAGE CONFORMS TO
A) JEDEC MS-001 VARIATION BA
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DIMENSIONS AND TOLERANCES PER
ASME Y14.5-1994
E) DRAWING FILE NAME: MKT-N14AREV7

Figure 3. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|---|--|--|----------------------------------|
| ACEx [®] | FPS [™] | PDP-SPM [™] | SupreMOS [™] |
| Build it Now [™] | FRFET [®] | Power220 [®] | SyncFET [™] |
| CorePLUS [™] | Global Power Resource SM | POWEREDGE [®] | SYSTEM [®] |
| CROSSVOLT [™] | Green FPS [™] | Power-SPM [™] | GENERAL [®] |
| CTL [™] | Green FPS [™] e-Series [™] | PowerTrench [®] | The Power Franchise [®] |
| Current Transfer Logic [™] | GTO [™] | Programmable Active Droop [™] | power [®] |
| EcoSPARK [®] | i-Lo [™] | QFET [®] | the franchise |
| EZSWITCH [™] * | IntelliMAX [™] | QS [™] | TinyBoost [™] |
|  | ISOPLANAR [™] | QT Optoelectronics [™] | TinyBuck [™] |
|  | MegaBuck [™] | Quiet Series [™] | TinyLogic [®] |
| Fairchild [®] | MICROCOUPLER [™] | RapidConfigure [™] | TINYOPTO [™] |
| Fairchild Semiconductor [®] | MicroFET [™] | SMART START [™] | TinyPower [™] |
| FACT Quiet Series [™] | MicroPak [™] | SPM [®] | TinyPWM [™] |
| FACT [®] | MillerDrive [™] | STEALTH [™] | TinyWire [™] |
| FAST [®] | Motion-SPM [™] | SuperFET [™] | µSerDes [™] |
| FastvCore [™] | OPTOLOGIC [®] | SuperSOT [™] 3 | UHC [®] |
| FlashWriter [®] * | OPTOPLANAR [®] | SuperSOT [™] 6 | Ultra FRFET [™] |
| | | SuperSOT [™] 8 | UniFET [™] |
| | | | VCS [™] |

* EZSWITCH[™] and FlashWriter[®] are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I33